ABSTRACT
SYNCHRONIZATION STATE DETECTOR

A system and method for reducing timing uncertainties in a serial data signal. A system may comprise a transmitter configured to transmit serial data to a receiver through a transmission medium, e.g., wireless, wired. The receiver may comprise an oscillator configured to generate multiple phases of a clock. The receiver may further comprise a retiming mechanism configured to reduce the timing uncertainties of the serial data received by the receiver by selecting a particular phase of the clock to be asserted to sample the serial data signal. The particular phase may be selected by selecting the appropriate synchronization state/retiming state. A retiming state indicates which particular phase of the clock should be asserted to sample the serial data signal. A synchronization state indicates which particular phase of the clock is the appropriate one to assert at a given transition of the serial data signal.

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